B5S16861

20-BIT TWO PORT BUS SWITCH

PRELIMINARY DATA

- HIGH SPEED: t_{PD} = 0.25ns (MAX.) at V_{CC} = 4.5V T_A=85°C
- ON RESISTANCE BETWEEN TWO PORT: 5Ω (TYP) at V_{CC} = 5.0V T_A=25°C
- LOW POWER DISSIPATION: I_{CC} = 1uA(MAX.) at T_A=25°C
- COMPATIBLE WITH TTL OUTPUTS: V_{IH}=2V(MIN), V_{IL}=0.8V(MAX)
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- OPERATING VOLTAGE RANGE: V_{CC}(OPR) = 4V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16861
- IMPROVED LATCH-UP IMMUNITY
- ESD PERFORMANCE: HBM > 2000V (MIL STD 883 method 3015); MM > 200V

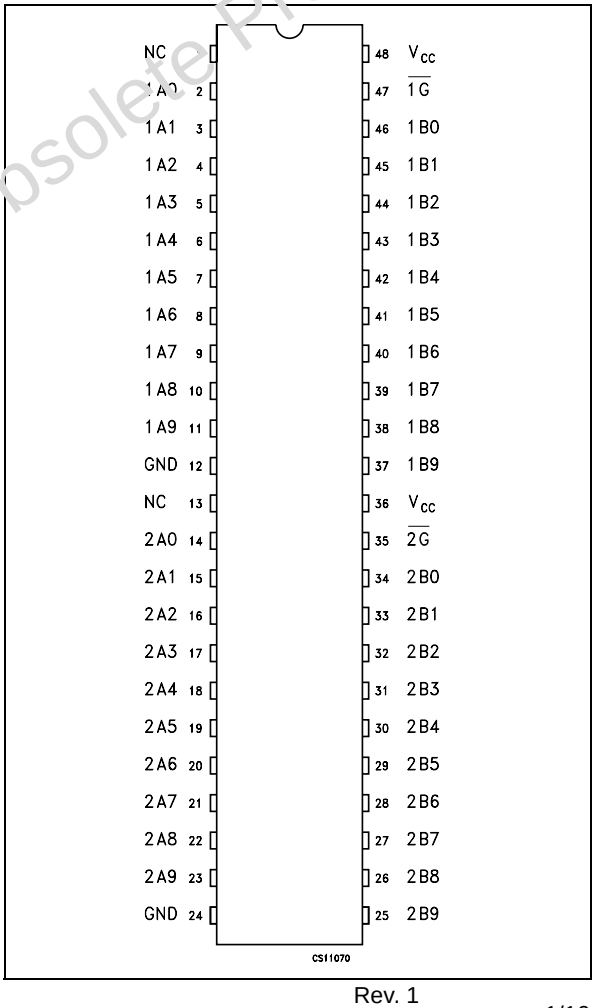


TSSOP

Table 1: Order Codes

PACKAGE	T & R
TSSOP48	B5S16861TTR

Figure 1: Pin Connection



DESCRIPTION

The B5S16861 is an advanced high-speed CMOS 20-BIT TWO PORT BUS SWITCH fabricated with sub-micron silicon gate and double-layer metal wiring C^2MOS technology.

It is ideal for 4V to 5.5V V_{CC} operations and ultra-low power and low noise applications, typically notebook and docking station.

Any $\overline{nG}$ output control governs two 10-bit BUS SWITCHES. Output Enable inputs ($\overline{nG}$) tied together gives full 20-bit operations. When $\overline{nG}$ is LOW, the switches are on. When $\overline{nG}$ is HIGH, the switches are in high impedance state.

It has ultra high-speed performance at 5V near zero delay with low ON resistance.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

Obsolete Product(s) - Obsolete Product(s)

This is preliminary information on a new product now in development are or undergoing evaluation. Details subject to change without notice.

Figure 2: Input Equivalent Circuit

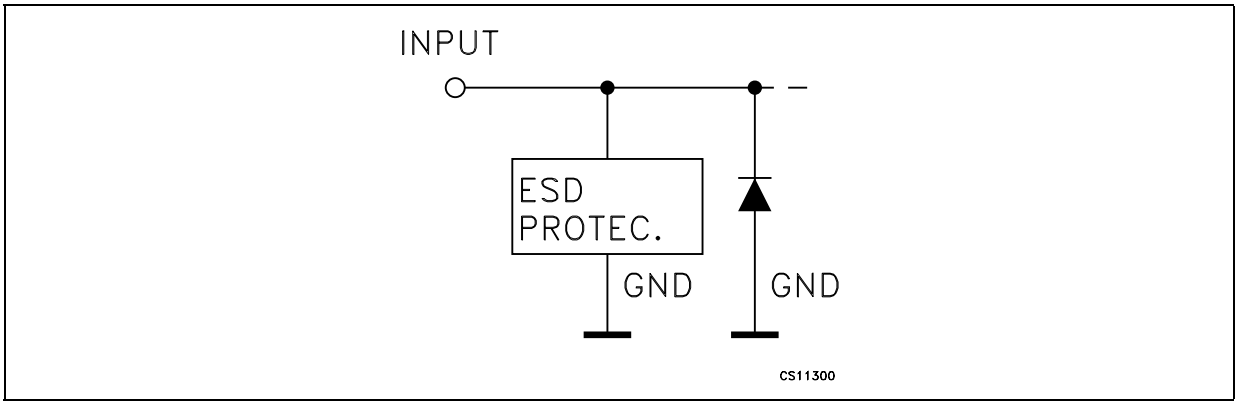


Table 2: Pin Description

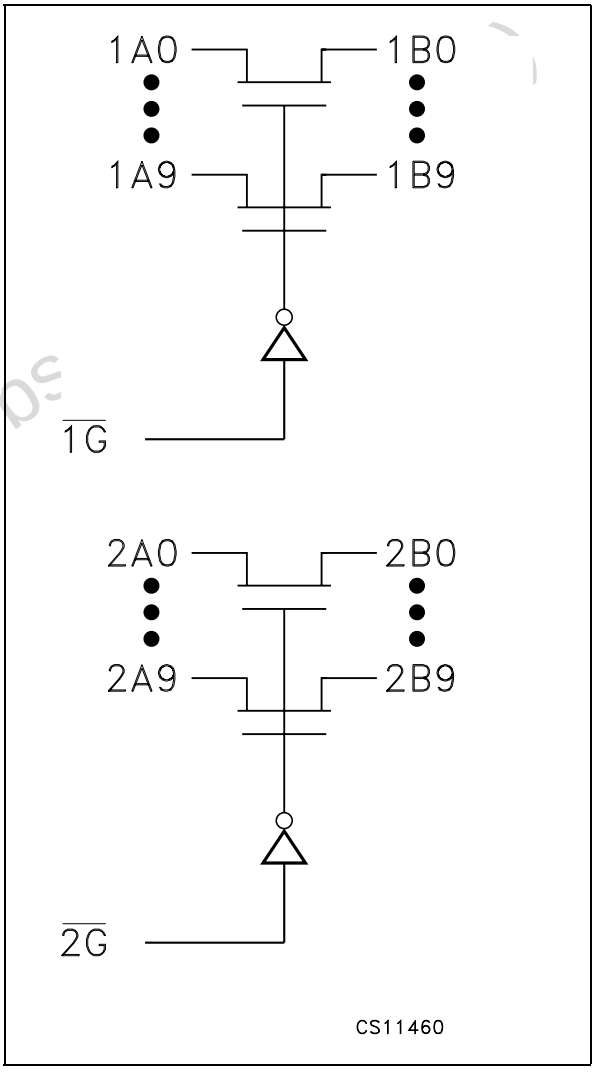
PIN N°	SYMBOL	NAME QND FUNCTION
1, 13	NC	Not Connected
2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1A0 to 1A9	Data Inputs
14, 15, 16, 17, 18, 19, 20, 21, 22, 23	2A0 to 2A9	Data Inputs
34, 33, 32, 31, 30, 29, 28, 27, 26, 25	2B0 to 2B9	Data Outputs
46, 45, 44, 43, 42, 41, 40, 39, 38, 37	1B0 to 1B9	Data Outputs
47, 35	$\overline{1G}$, $\overline{2G}$	Bus Enable Input (Active Low)
12, 24	GND	Ground (0V)
36, 48	V_{CC}	Positive Supply Voltage

Table 3: Truth Table

INPUT		OUTPUT
$\overline{nG}$	1An, 2An	1Bn, 2Bn
L	X	Bus ON
H	X	Z

n: 0 to 9
X: "H" or "L"
Z: High Impedance

Figure 3: Schematic Diagram



Obsolete Product(s) - Obs

Table 4: Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_I	DC Switch and Control Pin Voltage	-0.5 to +7.0	V
V_O	DC Output Voltage (V_{CC} = 0V) (note 1)	-0.5 to +7.0	V
V_O	DC Output Voltage ($V_{I/O}$=Gnd)	-0.5 to +7.0	V
I_{IK}	DC Input Diode Current ($V_{I/O}$ < 0V)	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current (note 3)	128	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Rating are those value beyond which damage to the device may occur. Functional operation under these condition is not implied
1) I_O absolute maximum rating must be observed
2) V_O < GND
3) Not more than one output should be tested at one time. Duration of the test should not exceed one second.

Table 5: Recommended Operating Conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4 to 5.5	V
V_I	Input Voltage	0 to 5.5	V
V_O	Output Voltage (V_{CC} = 0V)	0 to 5.5	V
V_O	Output Voltage	0 to 5.5	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Switch Input Rise and Fall Time	0 to DC	ns/V
dt/dv	Control Input Rise and Fall Time (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2V at V_{CC} = 3.0V

Obsolete Product(s) - Obsolete Product(s)

Table 6: DC Specification

Symbol	Parameter	Test Condition		Value							Unit
		V_{CC} (V)		T_A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	4 to 5.5		2			2		2		V
V_{IL}	Low Level Input Voltage	4 to 5.5				0.8		0.8		0.8	V
V_H	Input Hysteresis at Control pin	4.5 to 5.5			150						mV
R_{ON}	Switch ON Resistance	4.5	I_{ON}=64 mA V_I=0V					7			Ω
		4.5	I_{ON}=48 mA V_I=0V		5			7			
		4.5	I_{ON}=15 mA V_I=2.4V		10			15			
		4.0	I_{ON}=15 mA V_I=2.4V		14			22			
I_I	Input Leakage Current	0 to 5.5	V_I = 5.5V or GND			±0.1		±1.0		±2.0	µA
I_{OZ}	High Impedance Leakage Current	4.5 to 5.5	$V_{I/O}$ = 5.5V to GND					±1.0		±2.0	µA
V_{IK}	Clamp Diode Voltage	4.0 to 5.5	I_I = -18mA		-0.7			-1.2		-1.2	V
I_{CC}	Quiescent Supply Current	5.5	V_I = V_{CC} or GND		0.1	1.0		3.0		10.0	µA
I_{CCD}	Supply Current per Control Input per MHz (1)	5.5	$V_{I/O}$ = Open $\overline{nG}$=GND; Control Input Toggling 50% Duty Cycle					0.25			mA/ MHz
ΔI_{CC}	I_{CC} incr. per Input	5.5	V_{IC}=V_{CC}-2.1 V					2.5			mA

1) This current applies to the control inputs only and represent the current required to switch internal capacitance at the specified frequency. The 1An and 2An inputs generate no significant AC or DC currents as they transition. This parameter is not tested, but is guaranteed by design.

Table 7: AC Electrical Characteristics

Symbol	Parameter	Test Condition				Value				Unit
		V_{CC} (V)	C_L (pF)	R_L (Ω)	t_s = t_r (ns)	-40 to 85 °C		-55 to 125°C		
						Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time (1) xAn to xBn, xBn to xAn(2)	4.5 to 5.5	50	500	2.5		0.25			ns
t_{PZL} t_{PZH}	Output Enable Time		50	500	2.5	1.5	5.5			ns
t_{PLZ} t_{PHZ}	Output Disable Time		50	500	2.5	1.5	5.5			ns

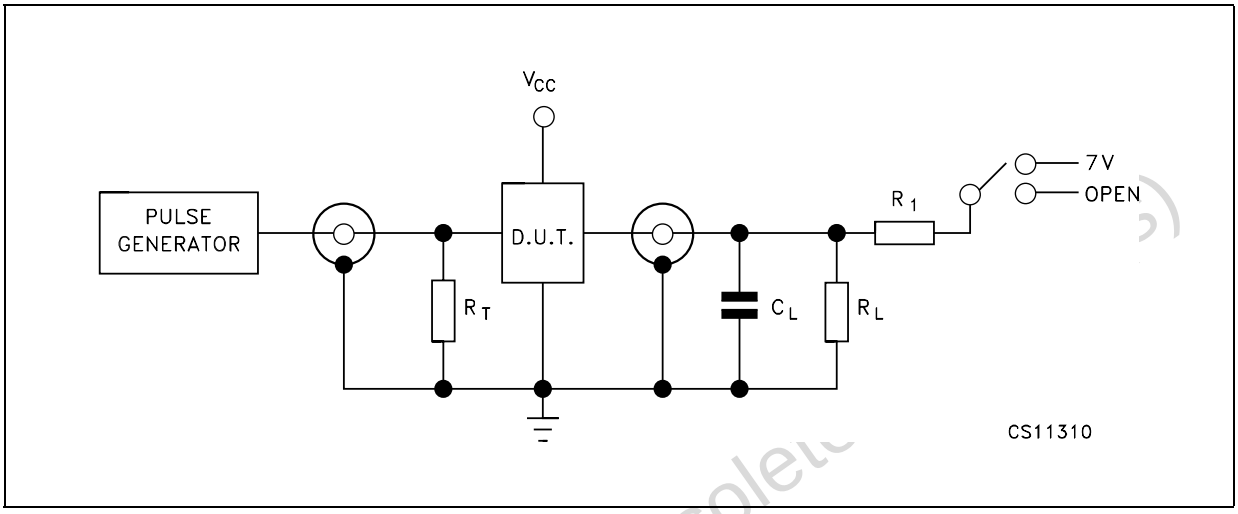
1) Parameter guaranteed by design
2) X=1,2; n=0..9.

Obsolete Product(s) - Obsolete Product(s)

Table 8: Capacitance Characteristics

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance at Control Pin				4		pF
$C_{I/O}$	Input Capacitance at I/O Pin	5.0	$\overline{nG}=V_{CC}$		5.5		pF

Figure 4: Test Circuit



TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	7V
t_{PZH}, t_{PHZ}	Open

C_L = 50pF or equivalent (includes jig and probe capacitance)
$R_L = R_1$ = 500Ω or equivalent
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Obsolete Product(s) - Obsolete

Figure 5: Waveform - Propagation Delay (f=1MHz; 50% duty cycle)

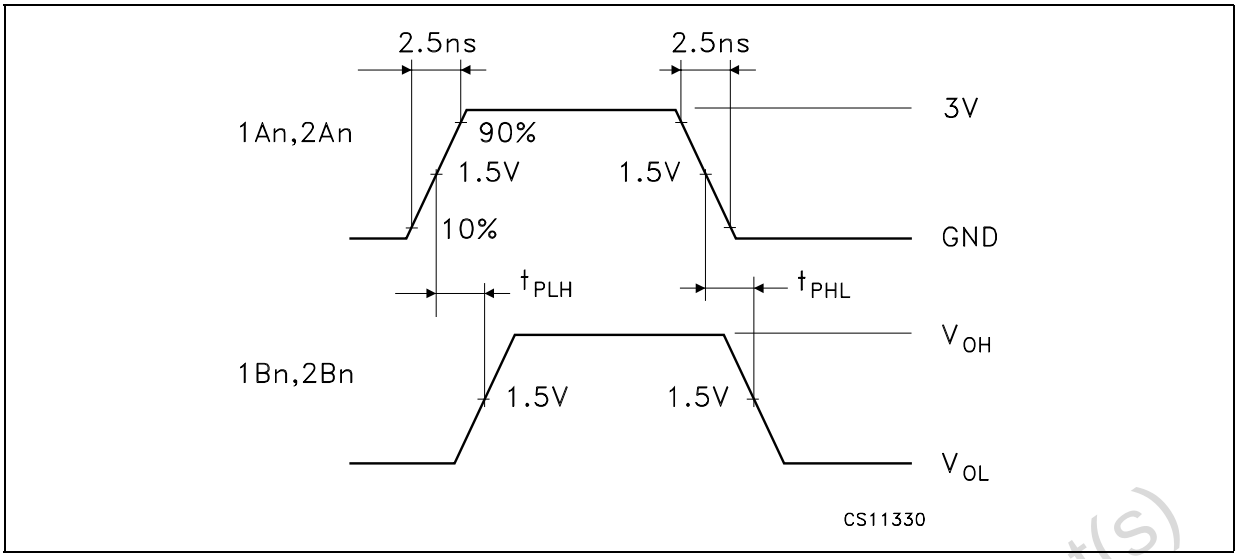
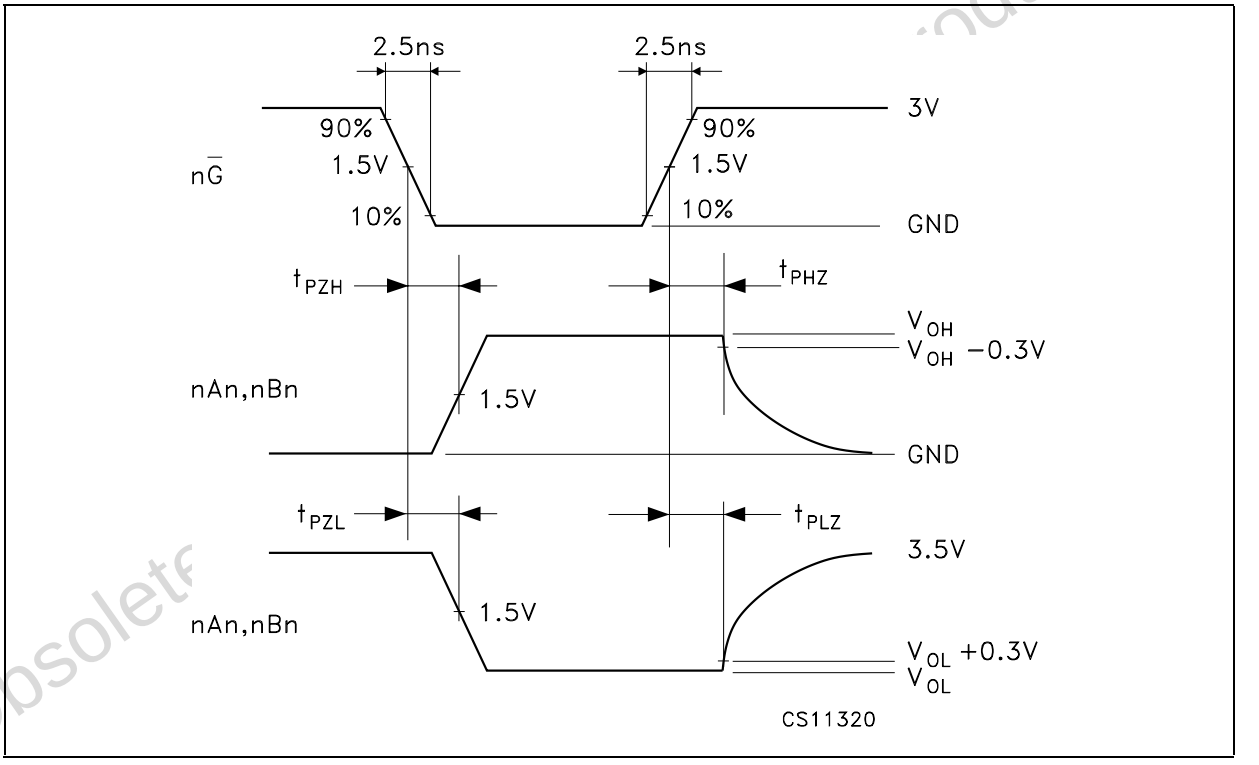


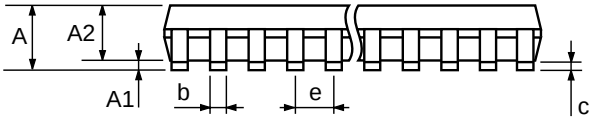
Figure 6: Waveform - Output Enable And Disable Time (f=1MHz; 50% duty cycle)

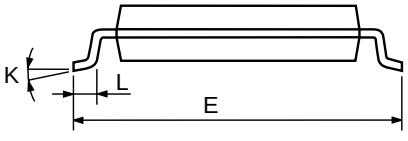


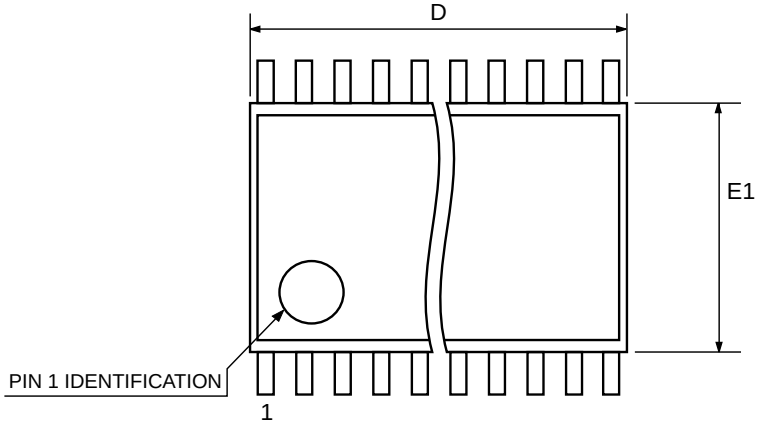
Obsolete Product(s)

TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.488		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.45		0.75	0.018		0.030



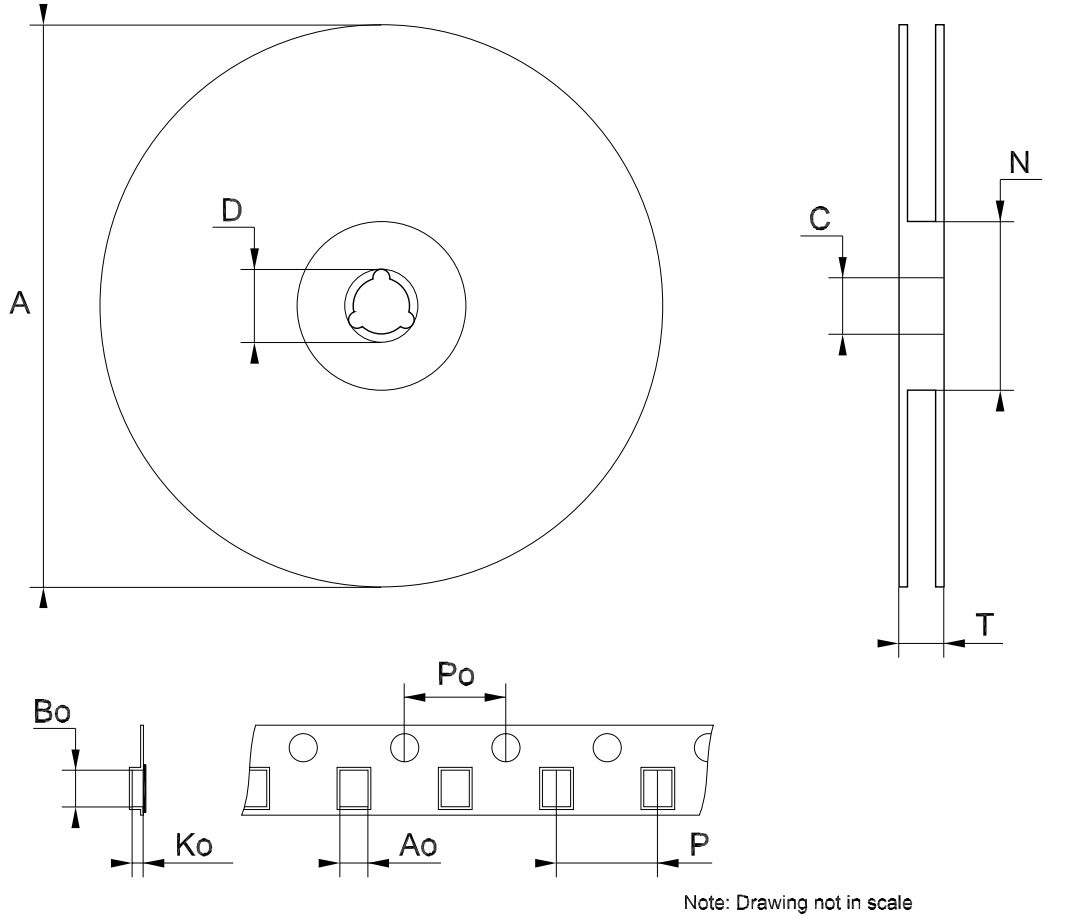




7065588D

Tape & Reel TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.343		0.350
Bo	13.1		13.3	0.516		0.524
Ko	1.5		1.7	0.059		0.067
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

Table 9: Revision History

Date	Revision	Description of Changes
01-Oct-2004	1	First Release.

Obsolete Product(s) - Obsolete Product(s)

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics

All other names are the property of their respective owners

© 2004 STMicroelectronics - All Rights Reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com